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U.S. UTILITY Patent Application

PATENT NUMBER and
ISSUE DATE

APPL NUM	FILING DATE	CLASS	SUBCLASS	GAU	EXAMINER
10038209	01/02/2002	716	6	2825	Thompson

**APPLICANTS: Rich Marvin; Misra Ashutosh;

**CONTINUING DATA VERIFIED:

NOUE

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** FOREIGN APPLICATIONS VERIFIED:

ADJSE

PG-PUB DO NOT PUBLISH ☐

RESCIND ☐

Foreign priority claimed

☐ yes ☒ no

35 USC 119 conditions met

☐ yes ☒ no

Verified and Acknowledged Examiner's initials

ATTORNEY DOCKET NO

POU920010165US1

TITLE : Delay correlation analysis and representation for vit compliant VHDL models

U.S. DEPT. OF COMM./PAT & TM-PTO-426L (Rev. 12-94)

NOTICE OF ALLOWANCE MAILED

Assistant Examiner

CLAIMS ALLOWED

Total Claims

Print Claim for
O.G.

ISSUE FEE

Amount Due

Date Paid

DRAWING

Sheets Drawg.

Figs. Drawg.

Print Fig.

Primary Examiner

PREPARED FOR ISSUE

Application Examiner



TERMINAL

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